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PTO/SB/21 (11-07)

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MP0390

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TDAMOLETTAL	Application Number	10/626,507		
TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Filing Date	July 24, 2003		
	First Named Inventor	Son Ho et al.		
	Art Unit	2188		
	Examiner Name	Kaushikkumar M. Patel		

Attorney Docket Number

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ENCLOSURES (check all that apply)						
Fee Transmittal F	- om	☐ Drawing(s)			After Allowance Communication to Technology Center (TC)	
Fee Attached	I	Licensing-r	elated Papers		Appeal Communication to Board of Appeals and Interferences	
Amendment / Re	ply	Petition			Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)	
After Final		Petition to Convert to a Provisional Application			Proprietary Information	
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Printed name	Michael D. Wiggins					
Date	June 30, 2008		Reg. No.	34,754		
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		First Named Inventor		Son Ho et	Son Ho et al.	
		Art Unit		2188		
		Examiner Name		Kaushikkumar M. Patel		
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	SIGNAT	TURE OF	APPLICANT, ATTO	ORNEY.	OR AGENT	
Firm Name	Harness, Dickey &					
Signature	Halil & Hoze					
Printed name	Michael D. Wiggins					
Date	June 30, 2008 Reg. No. 34,754					
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Signature Rachael a. O.			vermer		Date	June 30, 2008

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

	Appeal No				
Application No.:	10/626,507				
Filing Date:	July 24, 2003				
Appellants:	Son Ho et al.				
Conf. No.:	1965				
Group Art Unit:	2188				
Examiner:	Kaushikkumar Patel				
Title:	LINE CACHE CONTROLLER				

REPLY BRIEF TO EXAMINER'S ANSWER

Mail Stop Appeal Brief-Patents P.O. Box 1450 Alexandria, VA 22313-1450

June 30, 2008

Sir:

This reply brief is a reply to the Examiner's Answer mailed April 29, 2008, in the appeal from the decision of the Patent Examiner dated May 2, 2007, rejecting claims 1-28, 44-63, and 79-105, which are reproduced in Appendix A of this Appeal Brief.

STATUS OF THE CLAIMS

A statement identifying the status of the claims is contained in the Appeal Brief.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A statement identifying the grounds of rejection to be reviewed on appeal is contained in the Appeal Brief.

ARGUMENTS

Independent Claims 1, 12, 16, 19, 21, 44, 51, 55, 58, 59, 79, 90, 94, 96, and 98

With respect to claim 1, Appellants submit that Zaidi, either alone or in combination with any of the other cited prior art references, fails to show, teach, or suggest at least that said switch includes a plurality of selectors that each receive the second address and each select between first and second sets of signals relating to the first and second memory devices, respectively, based on the second address, and further submit that this structure is not inherent in the other cited prior art references.

As best understood by Appellants, Zaidi fails to disclose this limitation. Appellants respectfully note that the Examiner relies on a MAC (Media Access Controller) 140 to disclose the claimed switch and the plurality of selectors. Here again, Appellants respectfully submit that the MAC 140 does not necessarily include a plurality of selectors as Appellants' claims recite. In fact, Appellant respectfully notes that the MAC 140 does not selectively receive data based on switching, and instead receives all data over a "shared memory bus" 104. Typically, as known in the art, a MAC receives a data packet and routes the data based on an address field in the data packet. The Examiner still fails to provide any reference to support an allegation that the MAC 140 includes structure analogous to the plurality of selectors as the claims recite. The

Examiner relies on the MAC 140 to disclose the switch. Consequently, the MAC 140 must also include a plurality of selectors that each receive the second address and select between sets of signals based on the second address. Neither Zaidi nor any other cited prior art reference appears to suggest that the MAC 140 would include such a structure.

Attempting to make up for the deficiencies of Zaidi, the Examiner further notes that Jeddeloh discloses that a switch 160 "can be a set of multiplexers," and relies on Jeddeloh to support the assertion that the plurality of selectors would be inherent in the MAC 140 of Zaidi. Initially, Appellants respectfully note that that the claims recite that the plurality of selectors each receive the address and select between first and second sets of signals relating to first and second memory devices based on the address, and a mere reference to a set of multiplexers fails to disclose the specific structure of this limitation. The Examiner provides no evidence that the switch 160 of Jeddeloh includes a plurality of selectors that select between sets of signals based on a second address (i.e. an address in a memory select portion of an address signal).

Further, even if the alleged structure of Jeddeloh is analogous to the plurality of selectors in the present claims (which Appellants do not concede), Appellants respectfully note that the Examiner fails to provide any evidence whatsoever the that alleged structure of Jeddeloh would be inherently included in **a Media Access Controller**, specifically. Here again, a MAC generally views/receives all data packet traffic on a bus and directs the data packets according to address fields. A MAC, and in particular the MAC 140 as described in Zaidi, is not sometimes connected to one device and connected to another device at other times. Instead, the MAC 140 appears to be connected to both of the devices (e.g. flash 106 and SDRAM 108) at all times via the same interface (i.e. the **shared** bus 104). This structure is in complete contradiction to the structure of Appellants' claims, as well as the alleged "inherent" structure described in Jeddeloh.

Here again, Appellants note that the Examiner must show that the alleged structure **necessarily** (i.e. <u>must</u>) be included. Instead, the Examiner again cites optional structure included in Jeddeloh. In particular, Column 4, Lines 56-65 of Jeddeloh state merely that the "switch 160 can also be a set of multiplexers."

(Emphasis added). A recitation that a switch in Jeddeloh "can" or "may" be a set of multiplexers is in no way indicative that the MAC 140 of Zaidi necessarily includes a plurality of selectors as Appellants' claims recite.

Therefore, Appellants respectfully assert that the Examiner has failed to properly support his rejection under either 35 U.S.C. §103 and/or 35 U.S.C. §103 with an inherency argument. Appellants respectfully submit that Zaidi, either alone or in combination with Jeddeloh or any other cited reference, fails to disclose a plurality of selectors that each receive the address and select between first and second sets of signals relating to first and second memory devices based on the address. Appellants further submit that Examiner has failed to support his allegation that this structure is inherent in either Zaidi or Jeddeloh. Accordingly, Appellants respectfully submit that claim 1, as well as its dependent claims, are in condition for allowance for at least the above reasons. Claims 12, 16, 19, 21, 44, 51, 55, 58, 59, 79, 90, 94, 96, and 98, as well as their corresponding dependent claims, are in condition for allowance for at least similar reasons.

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Damian M. Aquino, Reg. No. 54,964, at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By:

Michael D. Wiggins Reg. No. 34,754 Damian M. Aquino Reg. No. 54,964

MDW/DMA/rao

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